A Dynamic Analog Concurrently-Processed Adaptive Chip

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Multivalued-to-Analog Converter

As a subcircuit of the refresh controller, the Multivalued-to-Analog Converter (M/AC) has an important role in the quantization and refresh of the analog signals, for a high-resolution output. Combining quantized signals without the use of an Analog-to-Digital Converter (ADC) and a Digital-to-Analog (DAC) is a new concept which has not been previously investigated. Use of this M/AC circuit is a more efficient use of expensive chip space, and an interesting new concept which may be useful in fuzzy-logic circuits, where analog is often instead of digital in data representation.

This circuit is first shown in the form of a resistor ladder (Figure 1), similar to the R-2R ladder which is often used in DACs.

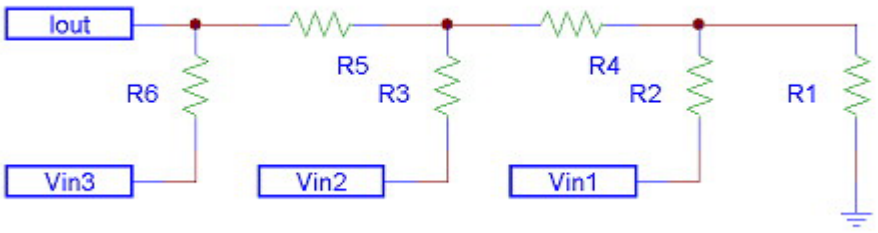

Figure 1: Basic M/AC or DAC resistor ladder

Assuming 4-bit resolution for each of V_{in1} and V_{in2}, we will also assume that $R_2 = R_3$, and $R_{tot}(R_1, R_2, R_4) = R_1$. This will make both voltage dividers R_2 R_1, and R_3 $R_{tot}(R_1, R_2, R_4)$ identical.

As a simplification to the following equations:

$$A = (R_{tot}(R_1, R_2) + R_4)/(R_3 + R_4 + R_{tot}(R_1, R_2)) \quad \textbf{(1)}$$

R_1 and R_2 must divide V_{in1} such that:

$$(1-A) \times (15/16 \times R_1/(R_1+R_2) + 1/16 \times R_1/(R_1+R_2)) = A \times 1/16 \quad \textbf{(2)}$$

$$(1-A) \times R_1/(R_1+R_2) = A \times 1/16 \quad \textbf{(3)}$$

Because the two voltage dividers are equivalent, A may be removed:

$$(1 - R_1/(R_1+R_2)) \times R_1/(R_1+R_2) = R_1/(R_1+R_2) \times 1/16 \quad \textbf{(4)}$$

$$R_2/(R_1+R_2) \times R_1/(R_1+R_2) = R_1/(R_1+R_2) \times 1/16 \quad \textbf{(5)}$$

$$R_2/(R_1+R_2) = 1/16 \quad \textbf{(6)}$$

This is to ensure the output level is linear, in that an input of:

$$[0001][0000] = A \times 1/16 \quad \textbf{(7)}$$

gives an output one level greater:

$$[0000][0001] = (1-A) \times R_1/(R_1 + R_2) \times 1/16 \quad \textbf{(8)}$$

than the input of:

$$[0000][1111] = (1-A) \times R_1/(R_1 + R_2) \times 15/16 \quad \textbf{(9)}$$

By arbitrarily setting $R_2 = R$, then R_1 can be solved to satisfy **(3)**:

$$R/(R_1+R) = 1/16 \quad \textbf{(10)}$$

$$16 \times R = R + R_1 \quad \textbf{(11)}$$

$$15 \times R = R_1 \quad \textbf{(12)}$$

Therefore, R_1 and R_2 have been found to be 15R and R respectively.

To solve the rest of the resistors, it is necessary to find the equivalent parallel resistance of R_1 and R_2:

$$R_{tot}(R_1, R_2) = 1 / ((1 / R_1) + (1 / R_2)) \quad \textbf{(13)}$$

$$R_{tot}(R_1, R_2) = 1 / ((1 / (15 \times R)) + (1 / R)) \quad \textbf{(14)}$$

$$R_{tot}(R_1, R_2) = 1 / ((1 / (15 \times R)) + (15 / (15 \times R))) \quad \textbf{(15)}$$

$$R_{tot}(R_1, R_2) = 1 / (16 / (15 \times R)) \quad \textbf{(16)}$$

$$R_{tot}(R_1, R_2) = 15/16 \times R \quad \textbf{(17)}$$

Due to the equivalency of the voltage dividers, the same ratio of 1/16 **(3)** must apply to:

$$R_3 / (R_3 + R_{tot}(R_1,R_2,R_4)) = 1/16 \quad \textbf{(18)}$$

$$R_3 / (R_3 + R_4 + 15/16 \times R) = 1/16 \quad \textbf{(19)}$$

Once again, R_3 may be arbitrarily set to R, yielding:

$$R / (R + R_4 + 15/16 \times R) = 1/16 \quad \textbf{(16)}$$

$$16 \times R = R + R_4 + 15/16 \times R \quad \textbf{(17)}$$

$$16 \times R - 15/16 \times R - R = R_4 \quad \textbf{(18)}$$

$$(14 + 1/16) \times R = R_4 \quad \textbf{(19)}$$

Then $R_1 = 15R$, $R_2 = R_3 = R$, and $R_4 = (14+1/16)R$.

If another 4-bit signal is to be used for V_{in3}, R_6 may be set to R, and R_5 to $(15+1/16)R$. However, the M/AC is not limited to combining signals of the same resolution. For example, V_{in3} may be a 3-bit signal. To combine this with the other signals, only R_5 and R_6 have to be recalculated.

As another simplification to the following equations:

$$B = (R_{tot}(R_1,R_2,R_3,R_4) + R_5)/(R_6 + R_5 + R_{tot}(R_1,R_2,R_3,R_4)) \quad \textbf{(20)}$$

$$(1 - B) \times A \times 15/16 + (1 - B) \times A \times 1/16 = B \times 1/8 \quad \textbf{(21)}$$

$$(1 - B) \times R_1/(R_1+R_2) = B \times 1/8 \quad \textbf{(22)}$$

$$(1 - B) \times 15R/(15R+R) = B \times 1/8 \quad \textbf{(23)}$$

$$(1 - B) \times 15/16 = B \times 1/8 \quad \textbf{(24)}$$

$$15/16 - B \times 15/16 = B \times 2/16 \quad \textbf{(25)}$$

$$15/16 = B \times 17/16 \quad \textbf{(26)}$$

$$15/17 = B \quad \textbf{(27)}$$

This is once again to ensure the output level is linear, in that an input of:

$$[001][0000][0000] = B \times 1/8 \quad \textbf{(28)}$$

gives an output one level greater:

$$[000][0001][0000] = (1 - B) \times A \times 1/16 \quad \textbf{(29)}$$

than the input of:

$$[000][1111][0000] = (1 - B) \times A \times 15/16 \quad \textbf{(30)}$$

Considering the total resistance of R1 – R4 is equivalent to that of R1 and R2, **(17)** may be used to calculate:

$$R_{tot}(R_1,R_2,R_3,R_4) = 15/16 \times R \quad \textbf{(31)}$$

Arbitrarily setting $R_6 = R$ yields:

$$B = (15/16 \times R + R_5)/(R + R_5 + 15/16 \times R) \quad \textbf{(32)}$$

Now, solving for R_5:

$$(15/16 \times R + R_5)/(R + R_5 + 15/16 \times R) = 15/17 \quad \textbf{(33)}$$

$$17 \times (15/16 \times R + R_5) = 15 \times (31/16 \times R + R_5) \quad \textbf{(34)}$$

$$17 \times 15/16 \times R + 17 \times R_5 = 15 \times 31/16 \times R + 15 \times R_5 \quad (35)$$

$$17 \times 15/16 \times R + 2 \times R_5 = 15 \times 31/16 \times R \quad (36)$$

$$17 \times 15 \times R + 32 \times R_5 = 15 \times 31 \times R \quad (37)$$

$$R_5 = 15 \times 14/32 \times R \quad (38)$$

$$R_5 = (6 + 9/16) \times R \quad (39)$$

Thus, R_5 may be set to $(6 + 9/16)R$ and R_6 to R to allow V_{in3} to be a 3-bit signal.

The complete M/AC circuit to combine two 4-bit signals with one 3-bit signal is shown in Figure 2.

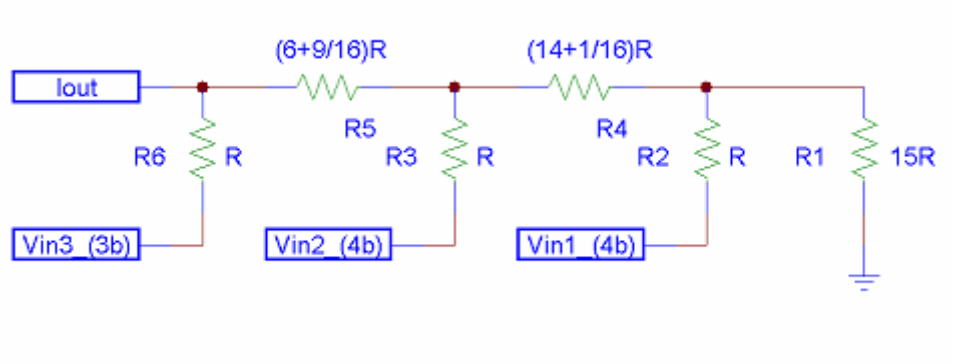

Figure 2: M/AC resistor ladder to combine two 4-bit and one 3-bit signals

An implementation of the M/AC may also take place using connected capacitors instead of resistors, for a lower-current voltage-mode output. In the CMOS process, compensation is required in this configuration to deal with parasitic capacitance to the substrate. Based on results from test runs of the TSMC 0.35um process over several years, mean parasitic capacitance was found to be 12.9% of the poly-oxide-poly capacitor (parasitic is poly-oxide-substrate), with standard deviation of 0.5%.