Comparison of
"A Dynamic Analog Concurrently-Processed Adaptive Chip"
vs.
"Electrically Trainable Analog Neural Network"

Feature	"A Dynamic Analog Concurrently-Processed Adaptive Chip" (Malcolm Stagg, 2006)	Electronically Trainable Artificial Neural Network (Intel, 1989)
On-Chip Learning	On-chip learning is fully implemented.	A computer must be connected for "chip-in-the-loop" learning.
Synapse Weight Volatility	Power must be applied. However, there is no limit on write cycles. Weights are stored to 12-bits, and stable to 4-bits.	Weights are stored with no power. However, write cycles are limited. Weights are stored to, and stable to 8-bits.
Stored Parameters	Synapse weights, individual learning rate parameters, and neuron average and deviance outputs are stored.	Only synapse weights are stored.
Density	Reasonably dense, requires more cells than the ETANN, but the newer chip technology (0.35um) allows smaller circuits.	Very dense. Not many cells are required for "chip-in-the-loop" learning. 1um chip technology is used.
Algorithmic Implementation	Hebbian and Backpropagation are implemented by default. A supervising controller may extend these algorithms.	Computer software contains several popular algorithms. No algorithms are implemented on-chip.
Analog Storage Capability	Supports high-resolution capacitor-based analog memory with a frequent quantization refresh	Supports analog memory based on floating-gate MOSFETs for permanent storage
Routability	A density of 8x8 routing pathways are implemented in SRAM for each neuron/synapse. Any neuron may be connected to any synapse. Any number of layers may be implemented.	Chip is not routable, but is fully-connected. A maximum of 2 layers of neurons can be implemented.
Expandability	Any number of chips can be connected together. The only limitation is packaging and bonding pads.	Any number of chips can be connected together. The only limitation is packaging and bonding pads.
Vital Cell Accuracy	Multipliers and sigmoid circuits are extremely accurate.	Multipliers are not linear over a wide range of inputs. Sigmoid has low accuracy.

Fully-Connected Capability	**It is not possible to connect all the neurons between two layers, unless the layers are very small.**	**Capable of being fully-connected with 2 layers of 64 neurons**
Inputs / Outputs	**Single-ended to conserve space. 16 inputs, 16 outputs for both forward- and backward- propagation. More are possible in a production chip. Outputs and inputs are interchangeable.**	**Single-ended to conserve space. 64 inputs, 64 outputs. No backwards-propagation connections due to "chip-in-the-loop" learning. Outputs may be used as inputs for large patterns.**
Supply Voltage	**A supply of 3.3V is required. This is enough voltage for reasonable accuracy.**	**A supply of 5V is required. In addition, a high voltage supply of about 20V is needed for programming synapse weights.**
Synapse to Neuron Density	**Test chip contains 3 synapses per neuron. 7, 15, 31, 63, etc… ratios are possible with minor design modifications.**	**64 synapses per neuron are implemented.**